Docket No.: M4065.0902/P902
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Peter P. Altice, Jr. et al.	Allowed: June 17, 2008
Application No.: 10/721,191	Confirmation No.: 6567
Filed: November 26, 2003	Art Unit: 2851
For: IMAGE SENSOR WITH A GATED STORAGE NODE LINKED TO TRANSFER GATE	Examiner: Not Yet Assigned

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE UNDER 37 CFR §1.104(E)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants have reviewed the Examiner's Statement of Reasons for Allowance with the June 17, 2008, Notice of Allowance and Allowability regarding the above-identified application. Entry of the Statement into the record should not be construed as any agreement with or acquiescence in the reasoning stated by the Examiner.

Applicants agree in part with the Examiner's Statement of Reasons for Allowance in that the prior art of record fails to anticipate or render obvious the claimed invention. However, Applicants note that the Examiner's statement fails to address all limitations of all of the allowed claims. Each of the claims stands on its own merits and is patentable because of the combination it recites and not because of the presence or absence of any one particular element. For example, certain claim limitations were not discussed in the Examiner's Reasons for Allowance, including

those in the dependent claims, each of which defines a unique combination of features not shown or suggested by the prior art, providing additional reasons for allowance of each claim.

Additionally, Applicants would like to clarify the Examiner's statement regarding claims 21, 30, 44 and 45. The Examiner's Comments state that these claims "require at least one barrier region separating a photosensor from a storage node *controlled by a transistor in the pixel*." (emphasis in original). Applicants note that Examiner's comment could be misunderstood as stating that the storage node is controlled by the transistor but that, per the claims, it is the barrier regions that are controlled by a respective one of the transistors.

The Examiner's Statement was not prepared by Applicants and only contains the Examiner's possible positions in one or more reasons for allowability. Thus, any interpretation with respect to the Examiner's Statement of Reasons for Allowance should not be imputed to the Applicants.

Dated: September 17, 2008

Respectfully submitted,

By_____

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